IN THE CLAIMS

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In the Claims:

1. (Original) A method of making chip stacks comprising the steps of:

providing a plurality of panels, each having a plurality of apertures therein and a plurality of conductive pads thereon;

providing a plurality of packaged chips having leads extending therefrom;

mounting the plurality of packaged chips within the plurality of apertures in the plurality of panels so that the leads thereof are disposed on at least some of the plurality of conductive pads on the plurality of panels;

assembling the plurality of panels into a panel stack;

soldering the leads of the packaged chips to at least some of the plurality of conductive pads and at least some of the conductive pads on adjacent panels together to form chip package stacks within the panel stack; and

separating the individual chip package stacks from the panel stack;

wherein one of the plurality of panels is scored to facilitate breaking of the panel between adjacent chip package stacks, and the remaining ones of the

plurality of panels have elongated slots therein to facilitate separation of adjacent chip package stacks; and

wherein said one of the plurality of panels is scored along a plurality of spaced-apart, parallel score lines which are perpendicular to the elongated slots in said remaining ones of the plurality of panels, and the step of separating the individual chip package stacks includes the steps of cutting through the panel stack along a plurality of spaced-apart, parallel lines which are perpendicular to the score lines, to form a plurality of strips of the chip package stacks, and within each strip breaking the strip along the score lines of a portion of said one of the plurality of panels within the strip to separate the individual chip package stacks from the strip.

2. (Original) A method of making chip stacks comprising the steps of:

providing a plurality of thin, planar panels, each having a plurality of apertures therein, a plurality of conductive pads on opposite surfaces of the panel adjacent each of the plurality of apertures, and a plurality of slots therein on opposite sides of each of the plurality of apertures;

mounting a different one of a plurality of packaged chips having leads within each of the plurality of apertures of each of the plurality of panels;

assembling the plurality of panels into a panel stack;

bonding the leads of the plurality of packaged chips to at least some of the plurality of conductive pads of the panels on which the packaged chips are mounted, and bonding at least some of the plurality of conductive pads of each panel to at least some of the conductive pads on at least one adjacent panel of the plurality of panels to form chip package stacks within the panel stack; and

cutting through each of the plurality of panels within the panel stack along lines perpendicular to the plurality of slots in each of the panels to separate the chip package stacks from the panel stack.

3. (Original) The method set forth in claim 2, wherein one of the plurality of thin, planar panels is formed without the plurality of slots therein and is broken following the cutting step to separate the chip package stacks.

4. (Original) The method set forth in claim 2, wherein the plurality of apertures in each panel are arranged into columns thereof extending along a length of the panel and rows thereof extending across a width of the panel and the plurality of slots in the panel are located between adjacent rows of the apertures.

5. (Original) The method set forth in claim 4, wherein the step of cutting is performed by cutting through each panel of the panel stack along the length of the panel adjacent opposite sides of the columns of apertures.

6. (Original) The method set forth in claim 2, wherein each of the plurality of apertures in each of the panels is of rectangular configuration so as to have four side edges which are surrounded by the conductive pads on each of the opposite sides of the panel, and each of the packaged chips comprises a thin, small outline chip package of rectangular configuration having plural leads extending from a pair of opposite side edges of the package and onto the conductive pads adjacent an opposite pair of side edges of an aperture in which the chip package is mounted, the chip package having a thickness like a thickness of the panel between opposite sides of the panel.

7. (New) A chip stack comprising:

at least two packaged chips, each of the packaged chips having opposite sides and a multiplicity of leads extending from each of the opposite sides thereof, and

at least one frame extending along at least each of the opposite sides of the packaged chips and comprising:

an upper surface having only first and second rows of conductive pads disposed thereon, each of the first and second rows of conductive pads extending along a respective one of the opposite sides of the packaged chips; and

a lower surface having only third and fourth rows of conductive pads disposed thereon, each of the third and fourth rows of conductive pads extending along a respective one of the opposite sides of the packaged chips;

each of the leads of one of the packaged chips being electrically connected to a respective one of the conductive pads of the first and second rows disposed on the upper surface of the frame, with each of the leads of one of the packaged chips being electrically connected to a respective one of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.

8. (New) The chip stack of Claim 7 wherein the packaged chips each comprise a TSOP packaged chip.

9. (New) The chip stack of Claim 7 wherein each of the conductive pads of the first and second rows disposed on the upper surface of the frame is

electrically connected to a respective one of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.

10. (New) A chip stack comprising:

two or more packaged chips arranged in a stack one above the other, each of the packaged chips having a first side, a second side opposite the first side, and a multiplicity of leads extending from each of the first side and the second side;

at least one framing structure having a first side frame portion extending along the first side of a selected one of the two or more packaged chips, a second side frame portion extending along the second side of the selected one, and two end frame portions, the first and second side frame portions and the end frame portions forming an aperture, a selected first one of the two or more packaged chips disposed at least partially in the aperture, the first side frame portion having an upper surface with a first row of conductive pads disposed therealong, and a lower surface with a second row of conductive pads disposed therealong, the second side frame portion having an upper surface with a third row of conductive pads disposed therealong, and a lower surface with a fourth row of conductive pads disposed therealong;

each of the leads of one of the packaged chips being electrically connected to a respective one of the conductive pads of the first and third rows of conductive pads, with each of the leads of the other of the packaged chips being electrically connected to a respective one of the conductive pads of the second and fourth rows of conductive pads.

11. (New) The chip stack of Claim 10 in which at least one of the conductive pads of the first row of conductive pads is electrically connected to a respective one of the conductive pads of the second row of conductive pads, and at least one of the conductive pads of the third row of conductive pads is electrically connected to a respective one of the conductive pads of the second row of conductive pads.

12. (New) The chip stack of Claim 10 in which the aperture has inner walls facing the selected first one of the two or more packaged chips, the inner walls being separated, by a gap, from the packaged chip along at least one side of the package chip.

13. (New) A chip stack comprising:two or more packaged chips arranged in a stack one above the other, each of the packaged chips having a

first side, a second side opposite the first side, and a multiplicity of leads extending from each of the first side and the second side;

a first side frame portion extending along the first side of a selected one of the two or more packaged chips, a second side frame portion extending along the second side of the selected one, the first side frame portion having an upper surface with a first row of conductive pads disposed therealong, and a lower surface with a second row of conductive pads disposed therealong, the second side frame portion having an upper surface with a third row of conductive pads disposed therealong, and a lower surface with a fourth row of conductive pads disposed therealong;

each of the leads of one of the packaged chips being electrically connected to a respective one of the conductive pads of the first and third rows of conductive pads, with each of the leads of the other of the packaged chips being electrically connected to a respective one of the conductive pads of the second and fourth rows of conductive pads.

14. (New) The chip stack of Claim 13 in which at least one of the conductive pads of the first row of conductive pads is electrically connected to a respective one of the conductive pads of the second row of conductive pads, and at least one of the conductive pads of the third row of conductive pads is

electrically connected to a respective one of the conductive pads of the second row of conductive pads.